

Fig. 1

Prior Art

High Level Design
Architecture

22

Floor Plan

Identify critical interconnects

Schematic Design - T-line topologies 30

24

Physical Design - T-lines as p-cells

26

Smart Extraction

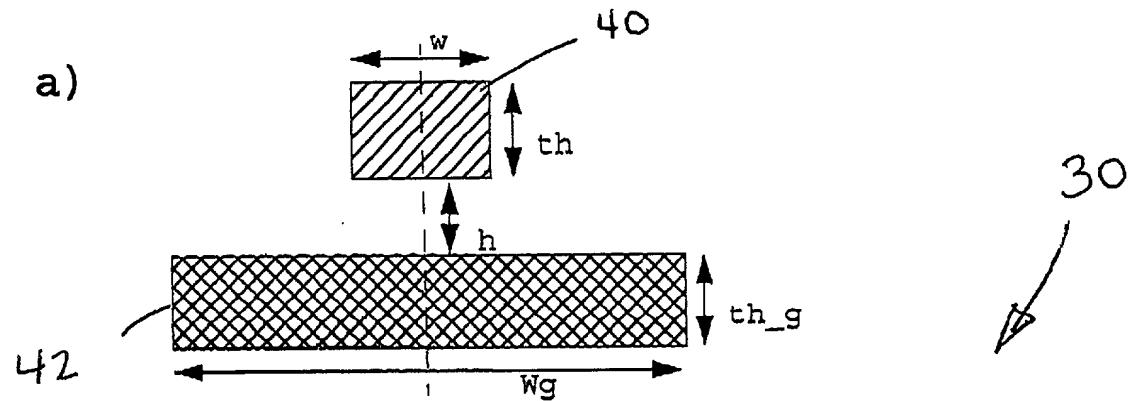
28

Final Simulation

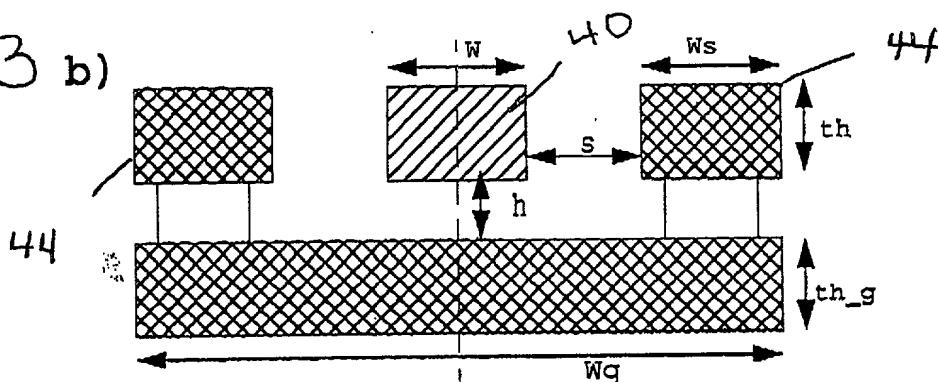
20

Fig. 2

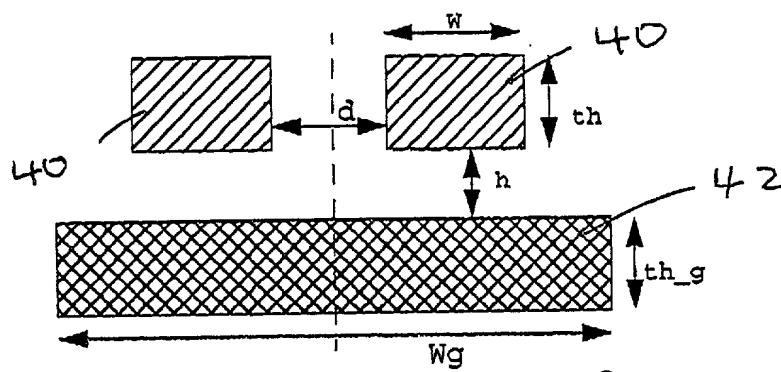
3 a)



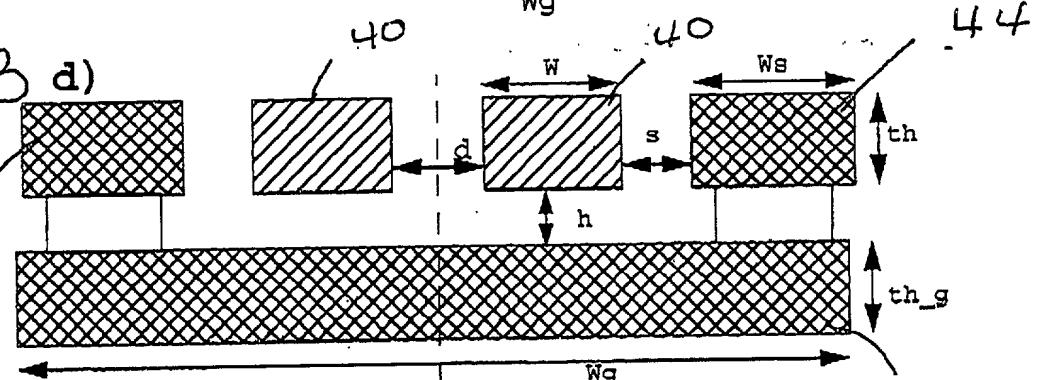
3 b)



3 c)



3 d)

Legend

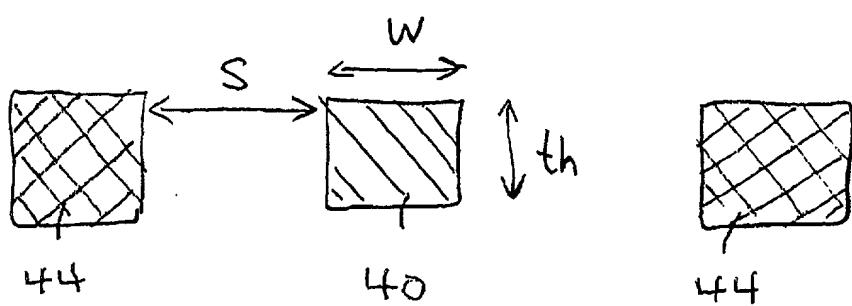
signal wire

shielding

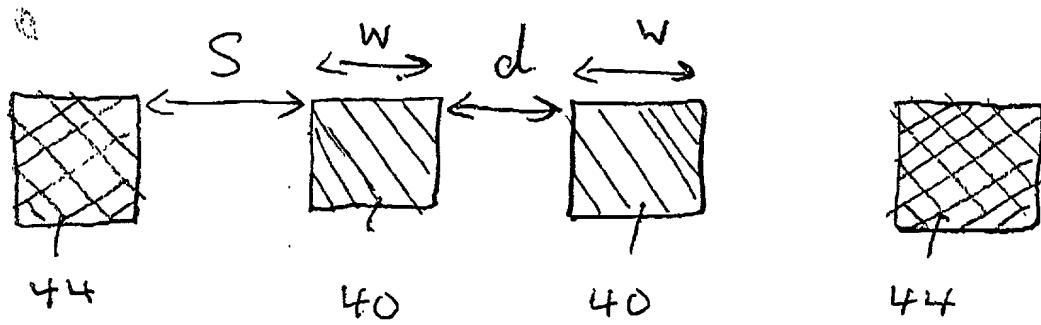
via

Figs. 3(a) - (d)

3e)



3f)



Figs. 3(e) - (f)

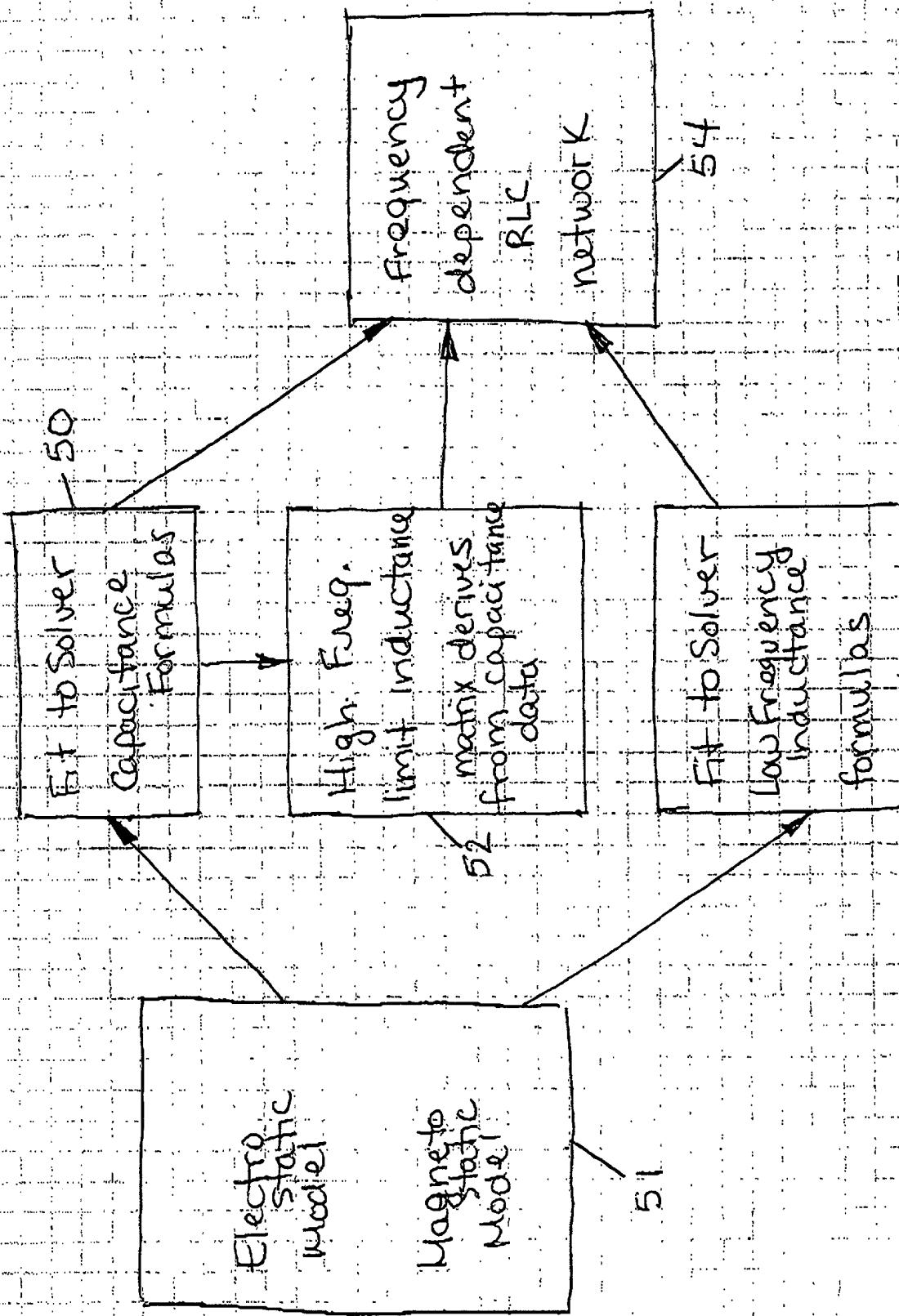


Fig. 4

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